TEA1733T; TEA1733LT

GreenChip III SMPS control IC Rev. 02 — 26 March 2010

Product data sheet

General description 1.

The TEA1733T and TEA1733LT are low cost Switched Mode Power Supply (SMPS) controller ICs intended for flyback topologies. The TEA1733(L) operates in fixed frequency mode. To reduce ElectroMagnetic Interference (EMI), frequency jitter has been implemented. Slope compensation is integrated for Continuous Conduction Mode (CCM) operation.

The TEA1733(L) IC incorporates OverPower Protection (OPP). This enables the controller to operate under overpower situations for a limited amount of time.

Two pins, VINSENSE and PROTECT, are reserved for protection purposes. Input UnderVoltage Protection (UVP) and OverVoltage Protection (OVP), output OVP and OverTemperature Protection (OTP) can be implemented using a minimal number of external components.

At low power levels, the primary peak current is set to 25 % of the maximum peak current and the switching frequency is reduced to limit switching losses. The combination of fixed frequency operation at high output power and frequency reduction at low output power provides high-efficiency over the total load range.

The TEA1733(L) enables low cost, highly efficient and reliable supplies for power requirements up to 75 W to be designed easily and with a minimum number of external components.

2. Features and benefits

2.1 Features

- SMPS controller IC enabling low-cost applications
- Large input voltage range (12 V to 30 V)
- Very low supply current during start-up and restart (typically 10 μA)
- Low supply current during normal operation (typically 0.5 mA without load)
- Overpower or high/low line compensation
- Adjustable overpower time-out
- Adjustable overpower restart timer
- Fixed switching frequency with frequency jitter to reduce EMI
- Frequency reduction with fixed minimum peak current to maintain high-efficiency at low output power levels
- Slope compensation for CCM operation
- Low and adjustable OverCurrent Protection (OCP) trip level
- Adjustable soft start operation



- Two protection inputs (e.g. for input UVP and OVP, OTP and output OVP)
- IC overtemperature protection

3. Applications

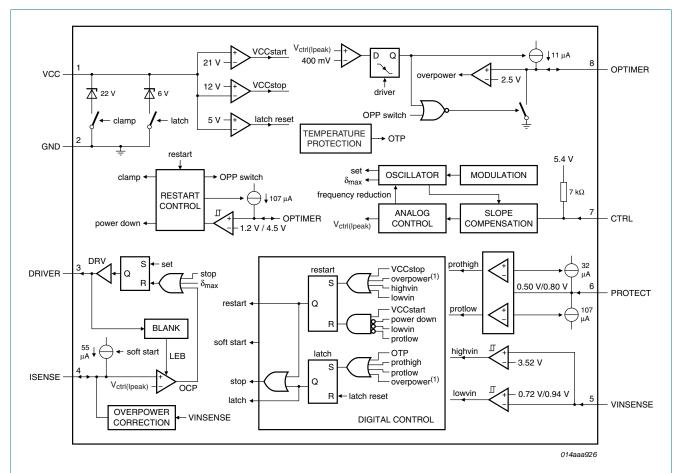
■ All applications requiring efficient and cost-effective power supply solutions to 75 W.

4. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|---------|---|---------|--|
| | Name | Description | Version | |
| TEA1733T | SO8 | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 | |
| TEA1733LT | SO8 | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 | |

5. Block diagram

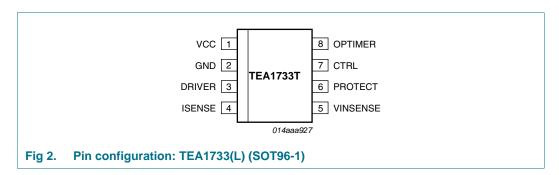


(1) In the TEA1733LT the Overpower signal switches the IC to the latched-off state. In the TEA1733T the Overpower signal triggers the restart timer.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

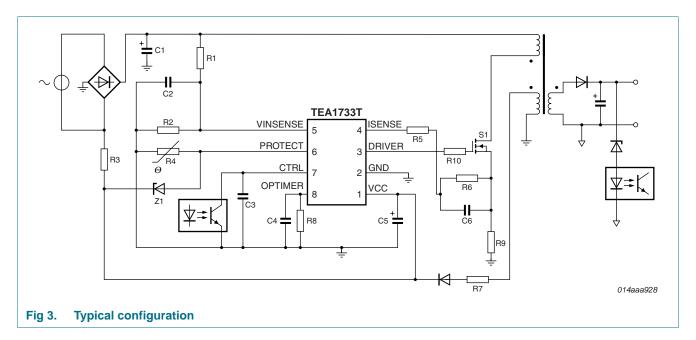
Table 2. Pin description

| Symbol | Pin | Description |
|----------|-----|----------------------------------|
| VCC | 1 | supply voltage |
| GND | 2 | ground |
| DRIVER | 3 | gate driver output |
| ISENSE | 4 | current sense input |
| VINSENSE | 5 | input voltage protection input |
| PROTECT | 6 | general purpose protection input |
| CTRL | 7 | control input |
| OPTIMER | 8 | overpower and restart timer |

7. Functional description

7.1 General control

The TEA1733(L) contains a flyback circuit controller, a typical configuration of which is shown in Figure 3.



7.2 Start-up and UnderVoltage LockOut (UVLO)

Initially, the capacitor on the VCC pin is charged from the high voltage mains via resistor R3.

If V_{CC} is lower than $V_{startup}$, the IC current consumption is low (typically 10 μ A). When V_{CC} reaches $V_{startup}$, the IC first waits for the VINSENSE pin to reach the $V_{start(VINSENSE)}$ voltage and PROTECT pin to reach the $V_{det(PROTECT)(L)}$ voltage. When both levels are reached, the IC charges the ISENSE pin to the $V_{start(soft)}$ level and starts switching. In a typical application the supply voltage is taken over by the auxiliary winding of the transformer.

If a protection is triggered the controller stops switching. Depending on the protection triggered and IC version (TEA1733T or TEA1733LT), the protection causes a restart or latches the converter to an off-state.

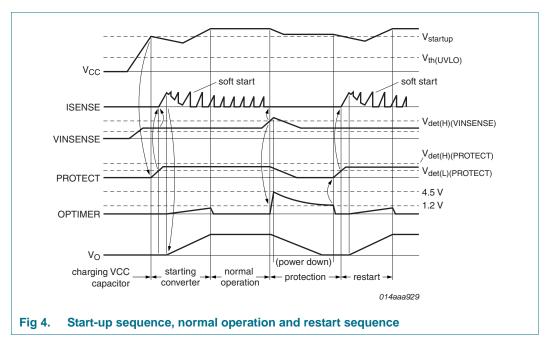
A restart caused by a protection rapidly charges the OPTIMER pin to 4.5 V (typical). The TEA1733(L) enters Power-down mode until the OPTIMER pin discharges down to 1.2 V (typical). In Power-down mode, the IC consumes a very low supply current (10 μ A typical) and the VCC pin is clamped at 22 V (typical) by an internal clamp circuit. When the voltage on pin OPTIMER drops below 1.2 V (typical) and the VCC pin voltage is above the VCC start-up voltage (See Figure 4), the IC restarts.

When a latched protection is triggered, the TEA1733(L) immediately enters Power-down mode. The VCC pin is clamped to a voltage just above the latch protection reset voltage $(V_{rst(latch)} + 1 V)$.

TEA1733T_TEA1733LT_2

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When the voltage on pin VCC drops below the UVLO level during normal operation, the controller stops switching and enters Restart mode. In Restart mode, the driver output is disabled and the VCC pin voltage is recharged via resistor R3 to the rectified mains.

7.3 Supply management

All internal reference voltages are derived from a temperature compensated on-chip band gap circuit. Internal reference currents are derived from a trimmed and temperature compensated current reference circuit.

7.4 Input voltage detection (VINSENSE pin)

In a typical application, the mains input voltage can be detected by the VINSENSE pin. Switching will not take place until the voltage on VINSENSE has reached the $V_{\text{start}(VINSENSE)}$ voltage (typically 0.94 V).

When the VINSENSE voltage drops below $V_{det(L)(VINSENSE)}$ (typically 0.72 V) or exceeds $V_{det(H)(VINSENSE)}$ (typically 3.52 V), the converter stops switching and performs a restart.

If pin VINSENSE is left open or disconnected, the pin is pulled up by the internal 20 nA (typical) current source to reach the $V_{det(H)(VINSENSE)}$ level. This triggers restart protection.

An internal clamp of 5.2 V (typical) protects this pin from excessive voltages.

7.5 Protection input (PROTECT PIN)

Pin PROTECT is a general purpose input pin, which can be used to switch off the converter (latched protection). The converter is stopped when the voltage on this pin is pulled above $V_{\text{det}(H)(PROTECT)}$ (typically 0.8 V) or below $V_{\text{det}(L)(PROTECT)}$ (typically 0.5 V). A current of 32 μA (typical) flows out of the chip when the pin voltage is at the $V_{\text{det}(L)(PROTECT)}$ level. A current of 107 μA (typical) flows into the chip when the pin voltage is at the $V_{\text{det}(H)(PROTECT)}$ level.

The PROTECT input can be used to create overvoltage detection and OTP functions.

A small 10 nF capacitor can be connected to the pin if the protections on this pin are not used.

An internal clamp of 4.1 V (typical) protects this pin from excessive voltages.

7.6 Duty cycle control (CTRL pin)

The output power of the converter is regulated by the CTRL pin. This pin is connected to an internal 5.4 V supply using an internal 7 $k\Omega$ resistor.

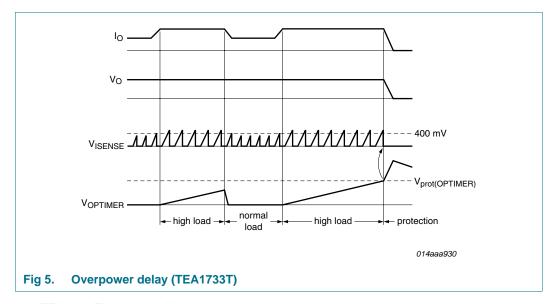
The CTRL pin voltage sets the peak current which is measured using the ISENSE pin (see Section 7.10). At a low output power, the switching frequency is also reduced (see Section 7.12). The maximum duty cycle is limited to 72 %.

7.7 Slope compensation (CTRL pin)

A slope compensation circuit is integrated in the IC or CCM. Slope compensation guarantees stable operation for duty cycles greater than 50 %.

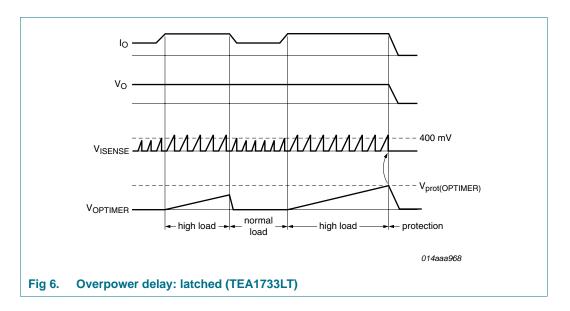
7.8 Overpower timer (OPTIMER pin)

If the OPTIMER pin is connected to capacitor C4 (see <u>Figure 3</u>), a temporary overload situation is allowed. $V_{ctrl(lpeak)}$ (see <u>Figure 1</u>) is set by the CTRL. When $V_{ctrl(lpeak)}$ is above 400 mV, the $I_{IO(OPTIMER)}$ current (11 μ A typical) is sourced from the OPTIMER pin. If the voltage on the OPTIMER pin reaches the $V_{prot(OPTIMER)}$ voltage (2.5 V typical) the OverPower Protection (OPP) is triggered (see <u>Figure 5</u>).



TEA1733T: when the V_{prot(OPTIMER)} voltage is reached the device restarted

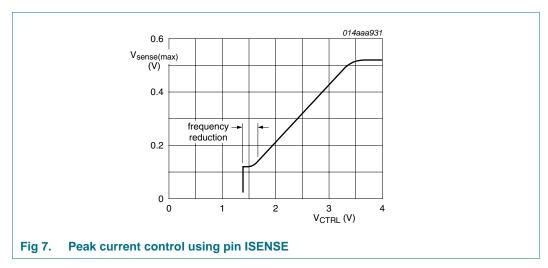
TEA1733LT: when the V_{prot(OPTIMER)} voltage is reached, it is latched in the off state



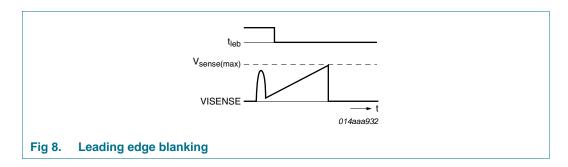
7.9 Current mode control (ISENSE pin)

Current mode control is used for its good line regulation.

The primary current is sensed by the ISENSE pin across an external resistor R9 (see <u>Figure 3</u>) and compared with an internal reference voltage. The internal reference voltage is proportional to the CTRL pin voltage (see <u>Figure 7</u>).



Leading edge blanking prevents false triggering due to capacitive discharge when switching on the external power switch (see Figure 8).

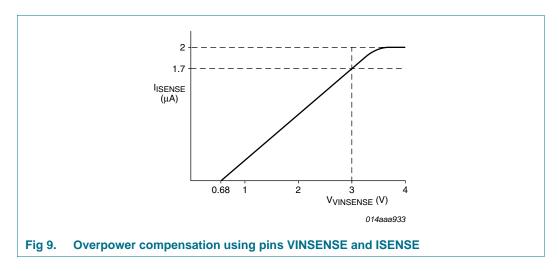


7.10 Overpower or high/low line compensation (VINSENSE and ISENSE pins)

The overpower compensation function can be used to realize a maximum output power which is nearly constant over the full input mains.

The overpower compensation circuit measures the input voltage on the VINSENSE pin and outputs a proportionally dependent current on the ISENSE pin. The DC voltage across the soft start resistor limits the maximum peak current on the current sense resistor.

At low output power levels, the overpower compensation circuit is switched off (See Figure 9).



7.11 Soft start-up (ISENSE pin)

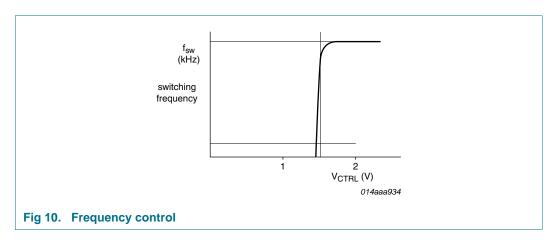
A soft start is made to prevent audible noise during start-up or a restart condition. Before the converter starts, the soft start capacitor C6 (see <u>Figure 3</u>) on the ISENSE pin is charged. When the converter starts switching, the primary peak current slowly increases as the soft start capacitor discharges through the soft start resistor (R6, see <u>Figure 3</u>).

The soft start time constant is set by the soft start capacitor value chosen. The soft start resistor value must also be taken into account, but this value is typically defined by the overpower compensation (see <u>Section 7.10</u>).

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7.12 Low power operation

In low power operation switching losses are reduced by lowering the switching frequency. The converter switching frequency is reduced and the peak current is set to 25 % of the maximum peak current (see Figure 7 and Figure 10).



7.13 Driver (pin DRIVER)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically -250 mA and a current sink capability of typically 750 mA. This allows for a fast turn-on and turn-off of the power MOSFET for efficient operation.

7.14 OverTemperature Protection (OTP)

Integrated overtemperature protection ensures the IC stops switching if the junction temperature exceeds the thermal temperature shutdown limit.

OTP is a latched protection and it can be reset by removing the voltage on pin VCC.

Limiting values 8.

Table 3. **Limiting values**

TEA1733T TEA1733LT 2

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------------------|--|-----------------|------|------|------|
| Voltages | | | | | |
| V _{CC} | supply voltage | continuous | -0.4 | +30 | V |
| | | t < 100 ms | - | 35 | V |
| V _{VINSENSE} | voltage on pin VINSENSE | current limited | -0.4 | +5.5 | V |
| V _{PROTECT} | voltage on pin PROTECT | current limited | -0.4 | +5 | V |
| V _{CTRL} | voltage on pin CTRL | | -0.4 | +5 | V |
| V _{IO(OPTIMER)} | input/output voltage on pin OPTIMER | | -0.4 | +5 | V |
| V _{ISENSE} | voltage on pin ISENSE | current limited | -0.4 | +5 | V |
| Currents | | | | | |
| I _{I(VINSENSE)} | input current on pin VINSENSE | | -1 | +1 | mA |
| I _{I(PROTECT)} | input current on pin PROTECT | | -1 | +1 | mA |

Table 3. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|---------------------------------|--------------------------|------------|------|------|
| I _{CTRL} | current on pin CTRL | | -3 | 0 | mA |
| I _{ISENSE} | current on pin ISENSE | | -10 | +1 | mA |
| I _{DRIVER} | current on pin DRIVER | δ < 10 % | -0.4 | +1 | Α |
| General | | | | | |
| P _{tot} | total power dissipation | T _{amb} < 75 °C | - | 0.5 | W |
| T _{stg} | storage temperature | | –55 | +150 | °C |
| T _j | junction temperature | | -40 | +150 | °C |
| ESD | | | | | |
| V _{ESD} | electrostatic discharge voltage | class 1 | | | |
| | | human body model | [1] - | 4000 | V |
| | | machine model | [2] - | 300 | V |
| | | charged device model | - | 750 | V |

^[1] Equivalent to discharging a 100 pF capacitor through a 1.5 $k\Omega$ series resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

| Symbol | Parameter | Conditions | Тур | Unit |
|----------------------|---|-------------------------------|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air; JEDEC test board | 150 | K/W |
| R _{th(j-c)} | thermal resistance from junction to case | in free air; JEDEC test board | 79 | K/W |

^[2] Equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω resistor.

10. Characteristics

Table 5. Characteristics

 T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

| Symbol | Parameter | Conditions | ı | Min | Тур | Max | Unit |
|-------------------------------|--|---|--------------|------|--------------------------|----------------|-------------------|
| Supply voltage r | management (pin VCC) | | | | | | |
| $V_{startup}$ | start-up voltage | | 1 | 18.6 | 20.6 | 22.6 | V |
| $V_{th(UVLO)}$ | undervoltage lockout threshold voltage | | 1 | 11.2 | 12.2 | 13.2 | V |
| V _{clamp(VCC)} | clamp voltage on pin | activated during restart | - | • | V _{startup} + 1 | - | V |
| | VCC | activated during latched protection | - | • | $V_{rst(latch)}$ + 1 | - | V |
| V _{hys} | hysteresis voltage | $V_{\text{startup}} - V_{\text{th(UVLO)}}$ | 8 | 3 | 9 | 10 | V |
| I _{CC(startup)} | start-up supply current | V _{CC} < V _{startup} | 5 | 5 | 10 | 15 | μΑ |
| I _{CC(oper)} | operating supply current | no load on pin DRIVER | C | 0.4 | 0.5 | 0.6 | mA |
| V _{rst(latch)} | latched reset voltage | | 2 | 4 | 5 | 6 | V |
| Input voltage se | nsing (pin VINSENSE) | | | | | | |
| V _{start(VINSENSE)} | start voltage on pin VINSENSE | detection level | (| 0.89 | 0.94 | 0.99 | V |
| V _{det(L)(VINSENSE)} | LOW-level detection voltage on pin VINSENSE | | (| 0.68 | 0.72 | 0.76 | V |
| V _{det(H)(VINSENSE)} | HIGH-level detection voltage on pin VINSENSE | | 3 | 3.39 | 3.52 | 3.65 | V |
| I _{O(VINSENSE)} | output current on pin VINSENSE | | - | - | -20 | - | nA |
| V _{clamp(VINSENSE)} | clamp voltage on pin VINSENSE | $I_{I(VINSENSE)} = 50 \mu A$ | - | • | 5.2 | - | V |
| Protection input | (pin PROTECT) | | | | | | |
| $V_{\text{det(L)(PROTECT)}}$ | LOW-level detection voltage on pin PROTECT | | (| 0.47 | 0.50 | 0.53 | V |
| V _{det(H)(PROTECT)} | HIGH-level detection voltage on pin PROTECT | | (| 0.75 | 0.8 | 0.85 | V |
| I _{O(PROTECT)} | output current on pin | $V_{VINSENSE} = V_{low(PROTECT)}$ | - | -34 | -32 | -30 | μΑ |
| | PROTECT | $V_{VINSENSE} = V_{high(PROTECT)}$ | 8 | 37 | 107 | 127 | μΑ |
| V _{clamp(PROTECT)} | clamp voltage on pin PROTECT | $I_{I(PROTECT)} = 200 \mu A$ | [1] 3 | 3.5 | 4.1 | 4.7 | V |
| Peak current co | ntrol (pin CTRL) | | | | | | |
| V_{CTRL} | voltage on pin CTRL | for minimum flyback peak current | 1 | 1.5 | 1.8 | 2.1 | V |
| | | for maximum flyback peak current | 3 | 3.4 | 3.9 | 4.3 | V |
| $R_{int(CTRL)}$ | internal resistance on pin CTRL | | 5 | 5 | 7 | 9 | kΩ |
| EA1733T_TEA1733LT_2 | All in | nformation provided in this document is subject to lega | ıl disclaime | rs. | | © NXP B.V. 201 | 0. All rights res |

 Table 5.
 Characteristics ...continued

 T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|-------------------------------------|--|--|-------|------------------------|-------|-------|
| O(CTRL) | output current on pin | V _{CTRL} = 1.4 V | -0.7 | -0.5 | -0.3 | mA |
| | CTRL | $V_{CTRL} = 3.7 V$ | -0.28 | -0.2 | -0.12 | mA |
| Pulse width mo | dulator | | | | | |
| osc | oscillator frequency | | 62 | 66.5 | 71 | kHz |
| f _{mod} | modulation frequency | | 210 | 280 | 350 | Hz |
| Δf_{mod} | modulation frequency variation | | ± 3 | ± 4 | ± 5 | kHz |
| $\delta_{\sf max}$ | maximum duty cycle | | 68.5 | 72 | 79 | % |
| V _{start(red)f} | frequency reduction start voltage | pin CTRL | 1.5 | 1.8 | 2.1 | V |
| $V_{\delta(zero)}$ | zero duty cycle voltage | pin CTRL | 1.25 | 1.55 | 1.85 | V |
| Overpower prot | ection (pin OPTIMER) | | | | | |
| $V_{prot(OPTIMER)}$ | protection voltage on pin OPTIMER | | 2.4 | 2.5 | 2.6 | V |
| I _{prot(OPTIMER)} | | no overpower situation | 100 | 150 | 200 | μΑ |
| | OPTIMER | overpower situation | -12.2 | -10.7 | -9.2 | μΑ |
| Restart timer (p | in OPTIMER) | | | | | |
| V _{restart(OPTIMER)} | restart voltage on pin | low level | 8.0 | 1.2 | 1.6 | V |
| | OPTIMER | high level | 4.1 | 4.5 | 4.9 | V |
| I _{restart} (OPTIMER) | restart current on pin OPTIMER | charging OPTIMER capacitor | -127 | -107 | -87 | μА |
| | | discharging OPTIMER capacitor | -0.1 | 0 | 0.1 | μА |
| Current sense (| pin ISENSE) | | | | | |
| V _{sense(max)} | maximum sense voltage | $\Delta V/\Delta t = 50 \text{ mV/}\mu\text{s};$ $V_{VINSENSE} = 0.78 \text{ V}$ | 0.48 | 0.51 | 0.54 | V |
| | | $\Delta V/\Delta t = 200 \text{ mV/}\mu\text{s};$ $V_{VINSENSE} = 0.78 \text{ V}$ | 0.50 | 0.53 | 0.56 | V |
| V _{th(sense)} opp | overpower protection sense threshold voltage | | 370 | 400 | 430 | mV |
| $\Delta V_{\text{ISENSE}}/\Delta t$ | slope compensation voltage on pin ISENSE | $\Delta V/\Delta t = 50 \text{ mV/}\mu\text{s}$ | 17 | 25 | 33 | mV/μs |
| t _{leb} | leading edge blanking time | | 250 | 300 | 350 | ns |
| Overpower com | pensation (pin VINSENSE | and pin ISENSE) | | | | |
| I _{opc(} ISENSE) | overpower compensation current on | V _{VINSENSE} = 1 V; V _{sense(max)} > 400 mV | - | 0.28 | - | μА |
| | pin ISENSE | V _{VINSENSE} =3 V; V _{sense(max)} > 400 mV | - | 1.7 | - | μΑ |
| Soft start (pin IS | SENSE) | | | | | |
| I _{start(soft)} | soft start current | | -63 | -55 | -47 | μΑ |
| | soft start voltage | V _{CTRL} = 4 V; enable | - | V _{sense(max} | | V |

 Table 5.
 Characteristics ...continued

 $T_{amb} = 25$ °C; $V_{CC} = 20$ V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|-----------------------------|--------------------------------------|----------------------------|------|------|-------|-----------|
| R _{start(soft)} | soft start resistance | | 12 | - | - | $k\Omega$ |
| Driver (pin DRI) | VER) | | | | | |
| I _{source(DRIVER)} | source current on pin DRIVER | V _{DRIVER} = 2 V | - | -0.3 | -0.25 | А |
| I _{sink(DRIVER)} | sink current on pin | V _{DRIVER} = 2 V | 0.25 | 0.3 | - | Α |
| | DRIVER | V _{DRIVER} = 10 V | 0.6 | 0.75 | - | Α |
| V _{O(DRIVER)max} | maximum output voltage on pin DRIVER | | 9 | 10.5 | 12 | V |
| Temperature pr | otection | | | | | |
| T _{pl(IC)} | IC protection level temperature | | 130 | 140 | 150 | °C |
| | | | | | | |

^[1] The clamp voltage on the PROTECT pin is lowered when the IC is in power-down (latched or restart protection).

11. Application information

A power supply with the TEA1733(L) is a flyback converter operating in Continuous conduction mode (See <u>Figure 11</u>).

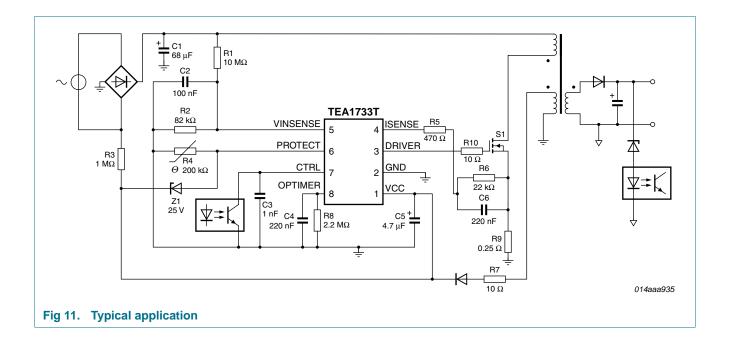
Capacitor C5 buffers the IC supply voltage, which is powered via resistor R3 at start-up and via the auxiliary winding during normal operation. Sense resistor R9 converts the current through the MOSFET S1 into a voltage on pin ISENSE. The value of R9 defines the maximum primary peak current on MOSFET S1. Resistor R7 reduces the peak current to capacitor C5.

In the example shown in Figure 11, the PROTECT pin is used for OVP and OTP. The OVP level is set by diode Z1 to V_{CC} = 25.8 V. The OTP level is set by Negative Temperature Coefficient (NTC) resistor R4. The VINSENSE pin is used for mains voltage detection and resistors R1 and R2 set the start voltage to about 80 V (AC). The overpower protection time is defined by capacitor C4 is set at 60 ms.

The restart time is defined by capacitor C4 and resistor R8 at 0.5 s.

Resistor R6 and capacitor C6 define the soft start time. Resistor R5 prevents the soft start capacitor C6 from being charged during normal operation caused by negative voltage spikes across the current sense resistor R9.

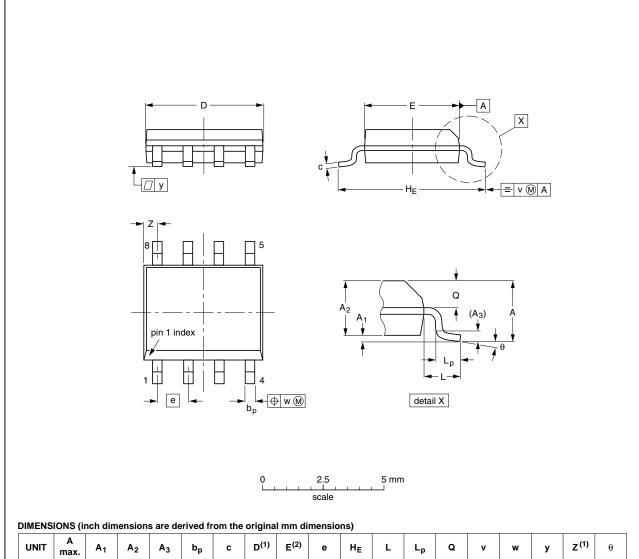
Capacitor C3 reduces noise on the CTRL pin.



12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



| UNIT | A max. | A ₁ | A ₂ | A ₃ | bp | С | D ⁽¹⁾ | E ⁽²⁾ | е | HE | ٦ | Lp | q | v | w | у | z ⁽¹⁾ | θ |
|--------|-----------|----------------|----------------|----------------|--------------|------------------|------------------|------------------|------|----------------|-------|----------------|----------------|------|------|-------|------------------|----|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 5.0 4.8 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° |
| inches | 0.069 | 0.010 0.004 | 0.057 0.049 | 0.01 | | 0.0100 0.0075 | 0.20 0.19 | 0.16 0.15 | 0.05 | 0.244 0.228 | 0.041 | 0.039 0.016 | 0.028 0.024 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | 0° |

Notes

- 1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
- 2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| | REFER | ENCES | EUROPEAN ISSUE DATE | | |
|--------|--------|-----------|---------------------|---------------------------------|--|
| IEC | JEDEC | JEITA | PROJECTION | ISSUE DATE | |
| 076E03 | MS-012 | | | 99-12-27 03-02-18 | |
| | | IEC JEDEC | IEC JEDEC JEITA | IEC JEDEC JEITA PROJECTION | |

Fig 12. Package outline SOT96-1 (SO8)

TEA1733T_TEA1733LT_2

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13. Revision history

Table 6. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes | | | | |
|----------------------|--|--|-----------------------|--------------------------------|--|--|--|--|
| TEA1733T_TEA1733LT_2 | 20100326 | Product data sheet | - | TEA1733T_TEA1733LT_1 | | | | |
| Modifications: | (VINSENS | Typical value of V_{start(VINSENSE)} changed in <u>Section 7.4 "Input voltage detection (VINSENSE pin)"</u>. | | | | | | |
| | Value of in | ternal voltage source change | ed in Section 7.6 "De | uty cycle control (CTRL pin)". | | | | |
| | Value of I_I | _{D(OPTIMER)} changed in <u>Section</u> | n 7.8 "Overpower tir | mer (OPTIMER pin)". | | | | |
| | Figure 6 "0" | Overpower delay: latched (TE | A1733LT)" added. | | | | | |
| | Pin numbe | er changed in <u>Table 5 "Chara</u> | cteristics". | | | | | |
| | • Figure 11 ' | Figure 11 "Typical application" changed. | | | | | | |
| | Package information in figure title of <u>Figure 12 "Package outline SOT96-1 (SO8)"</u> changed. | | | | | | | |
| TEA1733T_TEA1733LT_1 | 20091026 | Objective data sheet | - | - | | | | |

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14. Legal information

14.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|--------------------------------|-------------------|---|
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